AMENDMENTS TO THE CLAIMS:

Please add new claims 15 and 16 as follows:

1. (Previously Presented) A group III-nitride-based compound semiconductor device, comprising:

a first p-layer and a second p-layer, the first p-layer and the second p-layer comprising an acceptor impurity; and

an intermediate layer provided between the first p-layer and the second p-layer, the intermediate layer contacting a surface of the first p-layer and a surface of the second p-layer, the intermediate layer comprising a donor impurity,

wherein a concentration distribution of the donor impurity in the intermediate layer is based on activation rates of the acceptor and the donor impurities, such that at a specific temperature a compensation occurs to reduce a carrier concentration in said intermediate layer.

2. (Previously Presented) The group III-nitride-based compound semiconductor device according to claim 1, wherein:

the intermediate layer comprises a concentration distribution of donor impurity corresponding to a concentration distribution of the acceptor impurity in the intermediate layer.

3. (Previously Presented) The group III-nitride-based compound semiconductor device according to claim 1, wherein:

the acceptor impurity comprises magnesium and the donor impurity comprises silicon.

4. (Original) The group III-nitride-based compound semiconductor device according to claim 3, wherein:

the donor impurity of silicon has a concentration distribution substantially 1/10 that of the acceptor impurity of magnesium.

5. (Previously Presented) The group III-nitride-based compound semiconductor device according to claim 1, wherein:

the intermediate layer comprises a hole concentration equal to or less than $10^{17}/cm^3$.

6. (Original) The group III-nitride-based compound semiconductor device according to claim 1, wherein:

the first p-layer includes a p-cladding layer made of p-type AlGaN doped with Mg, and the second p-layer includes a p-contact layer made of p-type GaN doped with Mg.

7. (Previously Presented) A group III-nitride-based compound semiconductor device, comprising:

a sapphire substrate;

an n-contact layer formed on the sapphire substrate;

an n-cladding layer formed on the n-contact layer;

a light emitting layer formed on the n-cladding layer;

a p-cladding layer and a p-contact layer, to each of which an acceptor impurity is added;

an intermediate layer provided between the p-cladding layer and the p-contact layer, the intermediate layer contacting a surface of the p-cladding layer and a surface of the p-contact layer;

a thin film p-electrode disposed on the p-contact layer;

a thick film p-electrode disposed on the thin film p-electrode; and

an n-electrode disposed on the n-contact layer,

wherein a concentration distribution of the donor impurity in the intermediate layer is based on activation rates of the acceptor and the donor impurities, such that at a specific temperature a compensation occurs to reduce a carrier concentration in said intermediate layer.

8. (Original) The group III-nitride-based compound semiconductor device according to claim 7, wherein:

the light emitting layer includes a multiquantum well structure formed on the n-cladding layer by laminating multiple pairs of well layers of undoped InGaN and barrier layers of undoped GaN.

9. (Previously Presented) The group III-nitride-based compound semiconductor device according to claim 7, wherein:

the thin film p-electrode comprises a first layer of cobalt and a second layer of gold;

the thick film p-electrode is formed by laminating a first layer of vanadium, a second layer of gold, and a third layer of aluminum in sequence, on the thin film p-electrode; and

the n-electrode is formed by laminating a first layer of vanadium and a second layer of aluminum on a partly exposed portion of the n-contact layer.

10. (Original) The group III-nitride-based compound semiconductor device according to claim 7, further comprising:

a reflective metal layer of aluminum formed on the lower surface of the sapphire substrate.

11. (Previously Presented) A group III-nitride-based compound semiconductor device, comprising:

a first p-layer and a second p-layer, the first p-layer and the second p-layer comprising an acceptor impurity; and

an insulating layer provided between the first p-layer and the second p-layer, the insulating layer contacting a surface of the first p- layer and a surface of the second p-layer, the insulating layer comprising a donor impurity in a first concentration and the acceptor impurity in a second concentration,

wherein an amount of the donor impurity in the insulating layer offsets an activation rate of an amount of the acceptor impurity in the insulating layer.

12. (Previously Presented) The group III-nitride-based compound semiconductor device according to claim 11, wherein:

the insulating layer has a thickness of about 100 nm or less.

13. (Previously Presented) The group III-nitride-based compound semiconductor device according to claim 11, wherein:

the concentration of the donor impurity in the insulating layer in a thickness direction is substantially 1/10 of the concentration of acceptor impurity.

14. (Previously Presented) The group III-nitride-based compound semiconductor device according to claim 11, wherein:

an activation rate of the amount of the donor impurity is substantially equal to the activation rate of the amount of the acceptor impurity.

15. (New) The group III-nitride-based compound semiconductor device according to claim 1, wherein said first p-layer comprises $Al_{0.15}Ga_{0.85}N$.

16. (New) The group III-nitride-based compound semiconductor device according to claim 1, wherein said intermediate layer has a donor impurity concentration distribution of $2x10^{18}/cm^3$ to $3x10^{17}/cm^3$.